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RYAN, MASON & LEWIS, LLP
1300 POST ROAD, SUITE 205
FAIRFIELD,, CT 06430

EXAMINER	
DONAGHUE, LARRY D	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 09/538,755
Filing Date: March 30, 2000
Appellant(s): BERENBAUM ET AL.

Kevin M. Manson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/11/200

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-16 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,574,939	KECKLER ET AL.	11-1996
5,404,4699	CHUNG	4-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. . The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 6-9, and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (5,404,469).

3. Chung et al. taught a multithreaded VLIW (col. 5, lines 40-62) including a plurality of functional units (110) executing instructions grouped in packets by the compiler (col. 3, lines 8-29, col. 7, lines 20-40, col. 8, lines 32-55) and an allocator for selecting and forwarding the instructions to the functional units (col. 3, line 54 - col. 4, line 63, col. 3, lines 8-29, col. 7, lines 20-40, col. 8, lines 32-55) wherein the functional units can be allocated independently to any thread in the multithreaded instruction stream (col. 4, lines 11-63).

Chung et al. was cited by applicant on paper no. 3.

As to claims 8, 15 and 16, they fail to teach or define above or beyond claim 1, and are rejected for the reason set forth above.

As to claims 2 and 9, Chung et al. taught allocator assigns as many instructions as permitted by the availability of functional units (col. 3, lines 8-29).

As to claim to claims 6, 7, 13 and 14, Chung et al. taught the allocator can spilt an instruction packet (col. 3, line 54 - col. 4, line 63).

4. Claims 1-5, 8-12, and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Keckler et al.(5,574,939).

Keckler et al. was cited by applicant on paper no. 3.

Keckler et al. taught a multithreaded VLIW (abstract) including a plurality of functional units (250) executing instructions grouped in packets by the compiler (col. 1, lines 31-52) and an allocator for selecting and forwarding the instructions to the functional units (col. 2, lines 21-38, col. 3, line 58 - col. 4, line 8) and wherein the functional units can be allocated independently to any thread in the multithreaded instruction stream (col. 2, lines 21-37) .

As to claims 8, 15 and 16, they fail to teach or define above or beyond claim 1, and are rejected for the reason set forth above.

As to claims 2 and 9, Keckler et al. taught allocator assigns as many instructions as permitted by the availability of functional units (col. 2, lines 21-38).

As to claims 3 and 10, Keckler et al. taught storing the instruction for a later cycle (col. 9, line 56 - col. 10, line 18).

As to claims 4 and 11, Keckler et al. taught updating the instruction packets from the instruction stream of the thread (col. 9, line 56 - col. 10, line 18).

As to claims 5 and 12, Keckler et al. taught retaining the instruction packet (col. 9, line 56 - col. 10, line 18).

(11) Response to Argument

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the allocation of instructions in not done independently of the type of instruction ready for execution) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further see rejection for the details.

The allocation of instructions in not done independently of the type of instruction ready for execution is not disclosed. The cited portion of the specification "the illustrative Multithreaded VLIW processor 600 includes nine functional units 620-1 through 620-9, which can be allocated independently to any thread TA-TC." Does not mention that instruction are allocated independent of the type of instructions. The meaning of the phrased is defined in the specification page 10, lines 15-19; "In order to maximize, throughput across all threads, and minimize the number of cycles that a functional units rest idle, the present invention utilizes instruction packet splitting . Instead of allocating all operations in an instruction packet at one time, the allocation hardware 780, discussed above in conjunction with FIG. 8, assigns as many operations from each packet as will fit on the available functional units." The phrase, "the illustrative Multithreaded VLIW processor 600 includes nine functional units 620-1 through 620-9, which can be allocated independently to any thread TA-TC.", means that the functional units are not all assign to one packet, but can be spilt across multi-packet and each packet representing a different thread.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

LARRY D. DONAGHUE
PRIMARY EXAMINER

Ldd

March 30, 2004

Conferees

Andrew Caldwell
Andrew Caldwell

Patrice Winder
PATRICE WINDER
PRIMARY EXAMINER

RYAN, MASON & LEWIS, LLP
1300 POST ROAD, SUITE 205
FAIRFIELD,, CT 06430